Remarks

Applicant respectfully requests reconsideration of this application as amended. The specification has been amended to correct a minor informality. Claims 1, 5, 10, and 21 have been amended. Claims 31-33 have been added. No claims have been canceled. Claims 6, 17, and 28 were previously canceled. Therefore, claims 1-5, 7-16, 18-27, and 29-33 are presented for examination.

35 U.S.C. §102(e) Rejection

Claims 1-30 stand rejected under 35 U.S.C. §102(e) as being anticipated by Sih et al. (U.S. Patent No. 6,606,700). Applicant submits that the present claims are patentable over Sih.

Sih discloses a digital signal processor architecture that is designed to speed up frequently-used signal processing computations, such as FIR filters, correlations, FFTs, and DFTs. The architecture uses a coupled dual-MAC architecture and attaches a dual-MAC coprocessor onto it in such a way as to achieve an increase in processor capability. (Sih at col. 1, ll. 49-55.)

Claim 1, as amended, recites:

> A method comprising:
> receiving input data by an execution unit;
> performing, by the execution unit using a plurality of multiply-accumulate units in the execution unit, a plurality of current multiply-accumulate operations on the received input data; and
> saving the received input data for one or more multiply-accumulate operations to be performed by the execution unit after the current multiply-accumulate operation;
> wherein the performing a current multiply-accumulate operation includes:
> multiplying the received input data with a multiplier in the execution unit;
> adding an output from the multiplier with another value using an

adder in the execution unit; and

storing an output of the adder and providing the another value to the adder using an accumulator in the execution unit;

wherein the plurality of multiple-accumulate units are modular so that any number of multiply-accumulate units can be utilized proportionally for any given memory bandwidth.

First, applicant submits that Sih does not disclose or suggest saving the received input data for one or more multiply-accumulate operations to be performed by the execution unit after the current multiply-accumulate operation, as recited by claim 1. Sih at column 4, lines 28-31 states that "[t]o compute these four quantities simultaneously, the same coefficient h(k) is fed to all four multipliers simultaneously, while the other input is fed through a delay line to each of the multipliers." Yet, this cited portion of Sih only discloses ***simultaneous computation*** of four consecutive outputs. There is no disclosure or suggestion of saving a received input for a multiply-accumulate operation that are to be performed by an execution unit ***after a current multiply-accumulate operation***. Therefore, Sih does not disclose or suggest this cited feature of claim 1.

Second, application further submits that Sih does not disclose or suggest the plurality of multiple-accumulate units are modular so that any number of multiply-accumulate units can be utilized proportionally for any given memory bandwidth, as recited by claim 1. Applicant can find no disclosure or suggestion of such a feature anywhere in Sih. Therefore, Sih does not disclose or suggest this cited feature of claim 1.

Therefore, for the reasons discussed above, claim 1 is patentable over Sih. Claims 2-5, 7-9, and 31 depend from claim 1 and include additional limitations. Therefore, claims 2-5, 7-9, and 31 are also patentable over Sih.

Independent claims 10 and 21 also recite, in part, saving the received input data for one or more multiply-accumulate operations to be performed by the execution unit

after the current multiply-accumulate operation and the plurality of multiple-accumulate units are modular so that any number of multiply-accumulate units can be utilized proportionally for any given memory bandwidth. As discussed above, Sih does not disclose or suggest such a feature. Therefore, claims 10 and 21, as well as their respective dependent claims, are patentable over Sih for the reasons discussed above with respect to claim 1.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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